

CLAIMS

We claim:

1. A method of forming a capacitor, comprising the steps of:

providing a substrate having a lower low-k dielectric layer formed thereover;
the lower low-k dielectric layer having a dielectric constant of less than about 3.0;

forming metal vertical electrode plates within the lower low-k dielectric layer
5 such that adjacent metal vertical electrode plates have lower low-k dielectric layer
portions therebetween; and

replacing the lower low-k dielectric layer portions between the adjacent
metal vertical electrode plates with high-k dielectric material trench portions; the
high-k dielectric material trench portions having a dielectric constant of greater
10 than about 3.0.

2. The method of claim 1, wherein the substrate is a semiconductor wafer.

3. The method of claim 1, wherein the lower low-k dielectric layer has a thickness of
from about 2000 to 50,000Å.

4. The method of claim 1, wherein the lower low-k dielectric layer has a thickness of
from about 5000 to 10,000Å.

5. The method of claim 1, wherein the lower low-k dielectric layer is comprised of TEOS, FTEOS, Coral™, Black Diamond™ or an organic material.
6. The method of claim 1, wherein the lower low-k dielectric layer is comprised of an organic material.
7. The method of claim 1, wherein the high-k dielectric material trench portions are comprised of SiN, Ta_xO_y, Hf_xO_y, Ti_xO_y, Al₂O₃, Ta_xAl_yO_z, Ti_xAl_yO_z, SiO₂, Ta_xN_yO_z, Ti_xN_yO_z or a non-conductive oxidized refractory metal.
8. The method of claim 1, wherein the high-k dielectric material trench portions are comprised of a low leakage and high breakdown material.
9. The method of claim 1, wherein the high-k dielectric material trench portions have a dielectric constant of from about 7.0 to 50.0.
10. The method of claim 1, wherein the metal vertical electrode plates are comprised of copper or tungsten.
11. The method of claim 1, wherein the metal vertical electrode plates are comprised of copper.
12. The method of claim 1, including the step of lining the metal vertical electrode plates with respective metal barrier layers.

13. The method of claim 1, including the step of lining the metal vertical electrode plates with respective metal barrier layers comprised of Ta or TaN.

14. The method of claim 1, including the step of lining the metal vertical electrode plates with respective metal barrier layers comprised of Ta/TaN.

15. The method of claim 1, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

16. The method of claim 1, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective lined via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

17. The method of claim 1, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates to a thickness of from about 2000 to 50,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates; the via structures being comprised of copper or tungsten.

18. The method of claim 1, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates to a thickness of from about 5000 to 10,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates; the via structures being comprised of copper.

19. The method of claim 1, including the steps of:

forming an etch stop layer over the metal vertical electrode plates;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

20. The method of claim 1, including the steps of:

forming an etch stop layer over the metal vertical electrode plates to a thickness of from about 100 to 1000Å; the etch stop layer 100 being formed of SiN or $\text{Si}_x\text{O}_y\text{N}_z$;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

21. The method of claim 1, including the steps of:

forming an etch stop layer over the metal vertical electrode plates to a thickness of from about 300 to 600Å; the etch stop layer being formed of SiN;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

22. A method of forming a capacitor, comprising the steps of:

providing a substrate having a lower low-k dielectric layer formed thereover;
the lower low-k dielectric layer having a dielectric constant of less than about 3.0;

forming copper vertical electrode plates within the lower low-k dielectric
5 layer such that adjacent copper vertical electrode plates have lower low-k dielectric
layer portions therebetween; and

replacing the lower low-k dielectric layer portions between the adjacent
copper vertical electrode plates with high-k dielectric material trench portions; the
high-k dielectric material trench portions having a dielectric constant of greater
10 than about 3.0.

23. The method of claim 22, wherein the lower low-k dielectric layer has a thickness
of from about 2000 to 50,000Å.

24. The method of claim 22, wherein the lower low-k dielectric layer has a thickness
of from about 5000 to 10,000Å.

25. The method of claim 22, wherein the lower low-k dielectric layer is comprised of
TEOS, FTEOS, Coral™, Black Diamond™ or an organic material.

26. The method of claim 22, wherein the lower low-k dielectric layer is comprised of
an organic material.

27. The method of claim 22, wherein the high-k dielectric material trench portions are comprised of SiN, Ta_xO_y, Hf_xO_y, Ti_xO_y, Al₂O₃, Ta_xAl_yO_z, Ti_xAl_yO_z, SiO₂, Ta_xN_yO_z, Ti_xN_yO_z or a non-conductive oxidized refractory metal.

28. The method of claim 22, wherein the high-k dielectric material trench portions are comprised of a low leakage and high breakdown material.

29. The method of claim 22, wherein the high-k dielectric material trench portions have a dielectric constant of from about 7.0 to 50.0.

30. The method of claim 22, including the step of lining the copper vertical electrode plates with respective metal barrier layers.

31. The method of claim 22, including the step of lining the copper vertical electrode plates with respective metal barrier layers comprised of Ta or TaN.

32. The method of claim 22, including the step of lining the copper vertical electrode plates with respective metal barrier layers comprised of Ta/TaN.

33. The method of claim 22, including the steps of:

forming an upper low-k dielectric material layer over the copper vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates.

34. The method of claim 22, including the steps of:

forming an upper low-k dielectric material layer over the copper vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective lined via structures within the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates.

35. The method of claim 22, including the steps of:

forming an upper low-k dielectric material layer over the copper vertical electrode plates to a thickness of from about 2000 to 50,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates; the via structures being comprised of copper or tungsten.

36. The method of claim 22, including the steps of:

forming an upper low-k dielectric material layer over the copper vertical electrode plates to a thickness of from about 5000 to 10,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates; the via structures being comprised of copper.

37. The method of claim 22, including the steps of:

forming an etch stop layer over the copper vertical electrode plates;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates.

38. The method of claim 22, including the steps of:

forming an etch stop layer over the copper vertical electrode plates to a thickness of from about 100 to 1000Å; the etch stop layer 100 being formed of SiN or $\text{Si}_x\text{O}_y\text{N}_z$;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates.

39. The method of claim 22, including the steps of:

forming an etch stop layer over the copper vertical electrode plates to a thickness of from about 300 to 600Å; the etch stop layer being formed of SiN;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective copper vertical electrode plates.

40. A method of forming a capacitor, comprising the steps of:

providing a semiconductor wafer having a lower low-k dielectric layer formed thereover; the lower low-k dielectric layer having a dielectric constant of less than about 3.0 and a thickness of from about 2000 to 50,000Å;

5 forming metal vertical electrode plates within the lower low-k dielectric layer such that adjacent metal vertical electrode plates have lower low-k dielectric layer portions therebetween; the metal vertical electrode plates being comprised of copper or tungsten; and

10 replacing the lower low-k dielectric layer portions between the adjacent metal vertical electrode plates with high-k dielectric material trench portions; the high-k dielectric material trench portions having a dielectric constant of greater than about 3.0 and are comprised of a non-conductive oxidized refractory metal.

41. The method of claim 40, wherein the lower low-k dielectric layer has a thickness of from about 5000 to 10,000Å.

42. The method of claim 40, wherein the lower low-k dielectric layer is comprised of TEOS, FTEOS, Coral™, Black Diamond™ or an organic material.

43. The method of claim 40, wherein the lower low-k dielectric layer is comprised of an organic material.

44. The method of claim 40, wherein the high-k dielectric material trench portions are comprised of SiN, Ta_xO_y, Hf_xO_y, Ti_xO_y, Al₂O₃, Ta_xAl_yO_z, Ti_xAl_yO_z, SiO₂, Ta_xN_yO_z or Ti_xN_yO_z.

45. The method of claim 40, wherein the high-k dielectric material trench portions have a dielectric constant of from about 7.0 to 50.0.

46. The method of claim 40, wherein the metal vertical electrode plates are comprised of copper.

47. The method of claim 40, including the step of lining the metal vertical electrode plates with respective metal barrier layers.

48. The method of claim 40, including the step of lining the metal vertical electrode plates with respective metal barrier layers comprised of Ta or TaN.

49. The method of claim 40, including the step of lining the metal vertical electrode plates with respective metal barrier layers comprised of Ta/TaN.

50. The method of claim 40, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

51. The method of claim 40, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective lined via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

52. The method of claim 40, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates to a thickness of from about 2000 to 50,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates; the via structures being comprised of copper or tungsten.

53. The method of claim 40, including the steps of:

forming an upper low-k dielectric material layer over the metal vertical electrode plates to a thickness of from about 5000 to 10,000Å; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates; the via structures being comprised of copper.

54. The method of claim 40, including the steps of:

forming an etch stop layer over the metal vertical electrode plates;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

55. The method of claim 40, including the steps of:

forming an etch stop layer over the metal vertical electrode plates to a thickness of from about 100 to 1000Å; the etch stop layer 100 being formed of SiN or $\text{Si}_x\text{O}_y\text{N}_z$;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.

56. The method of claim 40, including the steps of:

forming an etch stop layer over the metal vertical electrode plates to a thickness of from about 300 to 600Å; the etch stop layer being formed of SiN;

forming an upper low-k dielectric material layer over the etch stop layer; the upper low-k dielectric material layer having a dielectric constant of less than about 3.0; and

forming respective via structures within the etch stop layer and the upper low-k dielectric material layer in electrical communication with the respective metal vertical electrode plates.